

## Course Description

This course introduces the UltraScale™ and UltraScale+™ architectures to both new and experienced designers.

The emphasis is on:

- Introducing CLB resources, clock management resources (MMCM and PLL), global and regional clocking resources, memory and DSP resources, and source-synchronous resources
- Describing improvements to the dedicated transceivers and Transceiver Wizard
- Reviewing the Memory Interface Generator (MIG) and DDR4 memory interface capabilities
- Migrating existing designs and IP to the UltraScale architecture with optimal use of the Vivado® Design Suite

### What's New for 2019.2

- HDL Coding Techniques: Auto-pipelining considerations

### Level – FPGA 3

**Course Duration** – 2 days

**Price** –

**Course Part Number** – FPGA-US

**Who Should Attend?** – Anyone who would like to build a design for the UltraScale or UltraScale+ device family

### Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- Intermediate VHDL or Verilog knowledge

### Software Tools

- Vivado HL Design or System Edition 2019.2

### Hardware

- Architecture: UltraScale and UltraScale+ FPGAs\*
- Demo board: None\*

\* This course focuses on the UltraScale and UltraScale+ architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary UltraScale architecture resources
- Describe the new CLB capabilities and the impact that they make on your HDL coding style
- Define the block RAM, FIFO, and DSP resources available
- Describe the new type of memory structures available in UltraScale+™ devices, such as UltraRAM and the high bandwidth memory (HBM) available in Virtex® UltraScale+ devices
- Properly design for the I/O and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included
- Identify the hard IP resources available for implementing high-performance DDR4 memory interfaces
- Describe the additional features of the dedicated transceivers
- Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

## Course Outline

### Day 1

- **Introduction to the UltraScale Architecture**  
Review the UltraScale architecture, which includes enhanced CLB resources, DSP resources, etc. {Lecture}
- **UltraScale Architecture CLB Resources**  
Examine the CLB resources, such as the LUT and the dedicated carry chain, in the UltraScale architecture. {Lecture, Lab}
- **HDL Coding Techniques**  
Covers basic digital coding guidelines used in an FPGA design. {Lecture, Lab}
- **UltraScale Architecture Clocking Resources**  
Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks. {Lectures, Lab}
- **FPGA Design Migration**  
Migrate an existing 7 series design to the UltraScale architecture. {Lecture, Lab}
- **Clocking Migration**  
Migrate a 7 series design to the UltraScale architecture with a focus on clocking resources. {Lab}
- **UltraScale Architecture Block RAM Memory Resources**  
Review the block RAM resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture FIFO Memory Resources**  
Review the FIFO resources in the UltraScale architecture. {Lecture}
- **UltraRAM Memory**  
Use UltraRAM for a design requiring a larger memory size than block RAM. {Lecture, Lab}
- **High Bandwidth Memory**  
Use high bandwidth memory (HBM) for applications requiring high bandwidth. {Lecture, Demo}

### Day 2

- **UltraScale Architecture DSP Resources**  
Review the DSP resources in the UltraScale architecture. {Lecture, Lab}
- **Design Migration Software Recommendations**  
List the Xilinx software recommendations for design migrations from 7 series to the UltraScale architecture. {Lecture}
- **DDR3 MIG Design Migration**  
Migrate a 7 series MIG design to the UltraScale architecture. {Lab}
- **DDR4 Design Creation Using MIG**  
Create a DDR4 memory controller with the Memory Interface Generator (MIG) utility. {Lab}
- **UltraScale Architecture I/O Resources Overview**  
Review the I/O resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture I/O Resources: Component Mode**  
Implement a high-performance, source-synchronous interface using I/O resources in Component mode for the UltraScale architecture. {Lecture, Lab}

- **UltraScale Architecture I/O Resources: Native Mode**  
Implement a high-performance, source-synchronous interface using I/O resources in Native mode for the UltraScale architecture. {Lecture, Lab}
- **Design Migration Methodology**  
Review the migration methodology recommended by Xilinx for design migrations. {Lecture}
- **10G PCS/PMA and MAC Design Migration**  
Migrate a successfully implemented 7 series design containing the 10G Ethernet MAC and 10G PCS/PMA IP to an UltraScale FPGA. {Lab}
- **UltraScale Architecture Transceivers**  
Review the enhanced features of the transceivers in the UltraScale architecture. {Lecture}
- **UltraScale FPGAs Transceivers Wizard**  
Use the Transceivers Wizard to build a design that uses a single serial transceiver and observe the created file structures. {Lecture, Demo, Lab}
- **Introduction to the UltraScale+ Families**  
Identify the enhancements made to the UltraScale architecture in the UltraScale+ architecture families. {Lecture}

## Register Today

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